ABSTRACT; For the abstract on page 14 of the specification, please make the following changes:

Delete page 14 as follows [An apparatus, system, and method to efficiently test a device under test by compression and decompression of test vectors and outputs.]

Replace with:

Logic to forward compressed test vectors to an IC, chipset, or SoC. Subsequently, the hardware decompresses the compressed test vectors and tests the IC, chipset, or SoC with the decompressed test vectors. The hardware has an option to bypass the compression of test vectors that are not efficiently compressed, such as, a data vector that actually increases in size after compression. As a result of the testing of the IC or SoC with test vectors, a plurality of outputs are generated by the IC, chipset, or SoC. The hardware also compresses the plurality of outputs generated by the IC or SoC, with an option to bypass the compression of outputs that are not efficiently compressed.